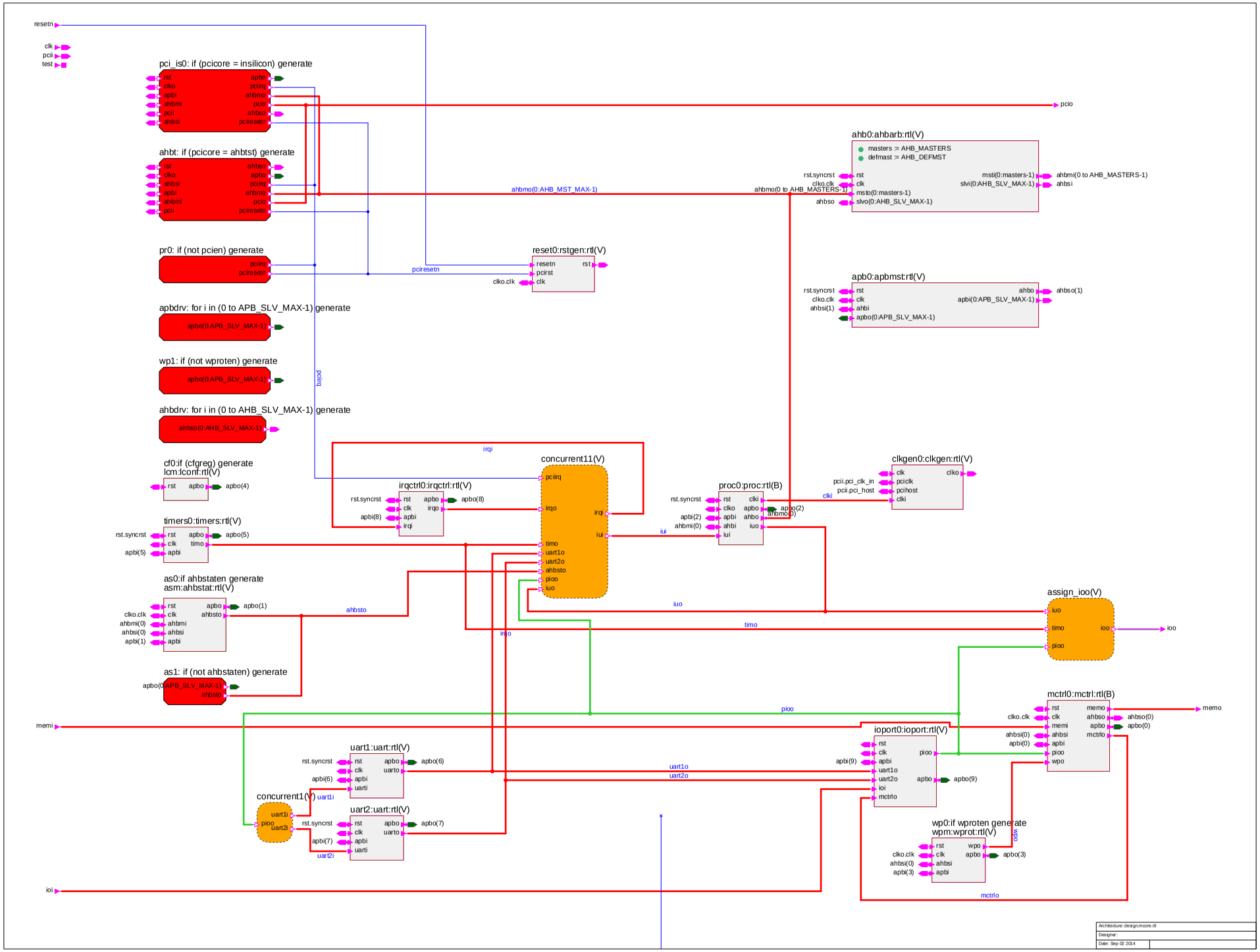
resetn
clk
pcii
test
pci_is0: if (pcicore = insilicon) generate
rst
clko
apbi
ahbmi
pcii
ahbsi
apbo
pciirq
ahbmo
pcio
ahbso
pciresetn
pcio
ahbt: if (pcicore = ahbtst) generate
ahbmo(0:AHB_MST_MAX-1)
ahb0:ahbarb:rtl(V)
masters := AHB_MASTERS
defmast := AHB_DEFMST
rst.syncrst
clko.clk
ahbmo(0 to AHB_MASTERS-1)
msti(0:masters-1)
slvi(0:AHB_SLV_MAX-1)
ahbmi(0 to AHB_MASTERS-1)
ahbsi
pr0: if (not pcien) generate
pciresetn
reset0:rstgen:rtl(V)
resetn
pcirst
apb0:apbmst:rtl(V)
ahbo
apbi(0:APB_SLV_MAX-1)
ahbso(1)
apbdrv: for i in (0 to APB_SLV_MAX-1) generate
apbo(0:APB_SLV_MAX-1)
wp1: if (not wproten) generate
pciirq
ahbdrv: for i in (0 to AHB_SLV_MAX-1) generate
ahbso(0:AHB_SLV_MAX-1)
irqi
concurrent11(V)
irqo
iui
timo
uart1o
uart2o
ahbsto
pioo
iuo
cf0:if (cfgreg) generate
lcm:lconf:rtl(V)
apbo(4)
irqctrl0:irqctrl:rtl(V)
apbo(8)
apbi(8)
clkgen0:clkgen:rtl(V)
clko
pciclk
pciihost
clki
pcii.pci_clk_in
pcii.pci_host
proc0:proc:rtl(B)
apbo(2)
ahbmo(0)
apbi(2)
ahbmi(0)
iui
timers0:timers:rtl(V)
apbo(5)
apbi(5)
as0:if ahbstaten generate
asm:ahbstat:rtl(V)
apbo(1)
ahbsi(0)
ahbsi(1)
ahbsto
assign_ioo(V)
ioo
as1: if (not ahbstaten) generate
apbo(0:APB_SLV_MAX-1)
mctrl0:mctrl:rtl(B)
memo
memi
ahbsi
mctrlo
wpo
ahbso(0)
apbo(0)
ioport0:ioport:rtl(V)
apbi(9)
apbo(9)
uart1:uart:rtl(V)
apbo(6)
apbi(6)
uarto
uarti
uart1i
concurrent1(V)
uart2:uart:rtl(V)
apbo(7)
apbi(7)
uart2i
wp0:if wproten generate
wpm:wprot:rtl(V)
apbo(3)
apbi(3)
ahbsi(0)
ioi
mctrlo
Architecture: designmcore.rtl
Designer:
Date: Sep 02 2014